4

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,561	10/14/2003	Mieu V. Vu	SC13003TH	4922

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EXAMINER	
FRANKLIN, RICHARD B	
ART UNIT	PAPER NUMBER
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/685,561	VU ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,12,15-23 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,12,15-23 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 5, 7, 12, 15 – 23 and 25 are pending.

Allowable Subject Matter

2. The indicated allowability of claims 6, 14 – 15 and 24 in the previous Office Action (mailed 20 September 2006) is withdrawn in view of the newly discovered reference(s) to "http://www.techfest.com/networking/wan/x25plp.htm" titled "X.25 Packet Layer Protocol (PLP) Overview" (hereinafter PLP). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 12, 15 – 18and 22 – 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 15 recites the limitation "an external interface bus" in lines 6 – 7 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if the limitation is referring to the "external interface bus" recited in the preamble of the claim or a new "external interface bus."

The Examiner has interpreted the limitation to refer to the "external interface bus" recited in the preamble.

5. Claim 22 recites the limitation "the controller means" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

The Examiner has interpreted the limitation to refer to "the controller" recited in claim 19.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 – 5, 7, 12, 19 – 22, and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,594,721 (hereinafter Pan) and "X.25 Packet Layer Protocol (PLP) Overview" (hereinafter PLP) (*PLP is used as extrinsic evidence to support a position of inherency*).

As per claim 1, Pan teaches a system having a processor (Pan; Figure 1 Item 18; Item 18 is the same as Figure 2 Item 62 which is described as a TouchTone™ phone (Pan; Col 4 Lines 45 – 47); TouchTone™ phones include a processor that makes the correct tone needed to complete the call) coupled to a system bus (Pan; Figure 1 Items 17, 22, 28, 30, and 32), a method of operating a device (Pan; Figure 1 Item 10), comprising instructing the processor to operate with the device (Pan; Col 4 Lines 25 – 28); putting information on the system bus (Pan; Col 4 Lines 25 – 28); retrieving the

information with a controller (Pan; Figure 1 Item 12); accessing a template of the device (Pan; Figure 1 Item 15, "CTP") with the controller responsive to the information (Pan; Col 3 Line 19 – 24, Col 4 Line 28 – 30); putting device information onto an external interface bus (Pan; Figure 1 Items 24 and 26) according to the information and the template (Pan; Col 4 Lines 30 – 33); and operating the device according to the device information (Pan; Col 6 Lines 53 – 55). Pan also teaches that the information includes an X.25 header (Pan; Figure 2 Items 68 and 78). X.25 headers inherently include a mode of operation (PLP; Section **X.25 Packet Header Format** "GENERAL FORMAT IDENTIFIER"), chip select (PLP; Section **X.25 Packet Header Format** "CHANNEL GROUP NUMBER"), access type (PLP; Section **X.25 Packet Header Format** "PACKET TYPE IDENTIFIER"), and an address (PLP; Section **X.25 Packet Header Format** "LOGICAL CHANNEL NUMBER"). Therefore, Pan inherently teaches that the information includes a mode of operation, chip select, access type, and an address.

As per claim 2, Pan also inherently teaches wherein the device is a peripheral with addressable registers or memory. The "subscriber" of Pan is described as a bank computer (Pan; Figure 2 Item 40). Addressable registers and memory are inherently included in a computer because they are fundamental to the operation of computers.

As per claim 3, Pan also inherently teaches wherein the system bus contains an address bus. Computer systems inherently include address busses in their system

busses. Address busses are used in combination with data busses to determine where to write data on the data busses.

As per claims 4 and 22, Pan also teaches wherein the information comprises a method of operation of the device. Pan teaches determining whether the information is an input message or an output message (Pan; Col 7 Lines 33 – 38).

As per claim 5, Pan also teaches wherein the method of operation is a read (Pan; Col 7 Lines 33 – 38, Col 7 Lines 50 – 67 "output message") or a write (Pan; Col 7 Lines 33 – 49 "input message").

As per claim 7, Pan also teaches wherein the template is selected from a plurality of templates (Pan; Col 3 Lines 15 – 24) stored in a memory (Pan; Figure 1 Item 14) coupled to the system bus (Pan; Figure 1 Items 17, 22, 28, 30, and 32), and wherein at least one template is optional on a per device type basis (Pan; Col 3 Lines 15 – 24). Before the system selects a specific template, all templates in the template database are options. A template is then selected based on the type of device (Pan; Col 3 Lines 15 – 24).

As per claim 19, Pan teaches a system comprising a processor (Pan; Figure 1 Item 18; Item 18 is the same as Figure 2 Item 62 which is described as a TouchTone™ phone (Pan; Col 4 Lines 45 – 47); TouchTone™ phones include a processor that makes

the correct tone needed to complete the call) coupled to a system bus (Pan; Figure 1 Items 17, 22, 28, 30, and 32); a memory coupled to the system bus (Pan; Figure 1 Item 14) for storing a plurality of templates (Pan; Figure 1 Item 15, "CTP"); and a controller (Pan; Figure 1 Item 12), coupled to the system bus and to an external interface bus (Pan; Figure 1 Items 24 and 26), wherein the controller is configured to retrieve a template of the plurality of templates in response to information received from the processor via the system bus (Pan; Col 4 Lines 25 – 33) and further configured to provide the information, in a manner consistent with the retrieved template, on the external interface bus (Pan; Col 4 Lines 25 – 33). Pan also teaches that the information includes an X.25 header (Pan; Figure 2 Items 68 and 78). X.25 headers inherently include a mode of operation (PLP; Section **X.25 Packet Header Format** "GENERAL FORMAT IDENTIFIER"), chip select (PLP; Section **X.25 Packet Header Format** "CHANNEL GROUP NUMBER"), access type (PLP; Section **X.25 Packet Header Format** "PACKET TYPE IDENTIFIER"), and an address (PLP; Section **X.25 Packet Header Format** "LOGICAL CHANNEL NUMBER"). Therefore, Pan inherently teaches that the information includes a mode of operation, chip select, access type, and an address.

As per claim 20, Pan also teaches wherein the template corresponds to the devices ID number (Pan; Col 3 Lines 56 – 60).

As per claim 21, Pan also teaches wherein the memory stores an operating system that identifies devices to be accessed (Pan; Col 3 Lines 11 – 15, Col 3 Line 65 – Col 4 Line 1, "advanced intelligent software package").

As per claim 23, Pan also inherently teaches wherein at least one of the templates is for a display controller because the device of Pan is a computer. It is well known in the art to have displays attached to computers in order to convey data or information to a user.

As per claim 25, Pan also teaches wherein the templates comprise access protocols of the devices (Pan; Col 2 Lines 21 – 24).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 12 and 15 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,594,721 (hereinafter Pan) and "X.25 Packet Layer Protocol (PLP) Overview" (hereinafter PLP) (*PLP is used as extrinsic evidence to support a position of inherency*) in view of the Examiner's taking of Official Notice.

As per claim 12, Pan teaches a system for controlling a device (Pan; Figure 1 Item 10) via an external interface bus (Pan; Figure 1 Items 24 and 26) comprising a processor (Pan; Figure 1 Item 18; Item 18 is the same as Figure 2 Item 62 which is described as a TouchTone™ phone (Pan; Col 4 Lines 45 – 47); TouchTone™ phones include a processor that makes the correct tone needed to complete the call) coupled to a system bus (Pan; Figure 1 Items 17, 22, 28, 30, and 32); a memory (Pan; Figure 1 Item 14) coupled to the system bus for storing templates (Pan; Figure 1 Item 15, "CTP") for describing operating characteristics of the devices (Pan; Col 3 Lines 15 – 24); and a controller (Pan; Figure 1 Item 12) coupled to the system bus and to an external interface bus. Pan also teaches that the information includes an X.25 header (Pan; Figure 2 Items 68 and 78). X.25 headers inherently include a mode of operation (PLP; Section **X.25 Packet Header Format** "GENERAL FORMAT IDENTIFIER"), chip select (PLP; Section **X.25 Packet Header Format** "CHANNEL GROUP NUMBER"), access type

(PLP; Section **X.25 Packet Header Format** "PACKET TYPE IDENTIFIER"), and an address (PLP; Section **X.25 Packet Header Format** "LOGICAL CHANNEL NUMBER"). Therefore, Pan inherently teaches that the information includes a mode of operation, chip select, access type, and an address. Pan also teaches wherein the controller receives information from the processor via the system bus (Pan; Col 4 Lines 25 – 27) and that the templates are stored on a disk memory (Pan; Figure 1 Item 14).

Pan does not teach receiving templates from the memory via the system bus.

However, the Examiner has taken Official Notice that it would have been obvious to have moved the memory to the system bus.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Pan to include moving the memory of Pan to the system bus because doing so would allow for other devices connected to the system bus to use and modify the contents of the memory.

As per claim 15, Pan also teaches wherein the templates comprise data about the operating characteristics of the devices (Col 3 Lines 24 – 27).

As per claim 16, Pan also teaches wherein the templates comprise access protocols of the devices (Col 2 Lines 21 – 24).

As per claim 17, Pan obviously teaches wherein at least one of the templates is for a display controller because the device of Pan is a computer. It is well known in the

art to have displays attached to computers in order to convey data or information to a user.

As per claim 18, Pan also obviously teaches wherein the system bus contains an address bus. Computer systems inherently include address busses in their system busses. Address busses are used in combination with data busses to determine where to write data on the data busses.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Franklin
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Art Unit 2181

DONALD SPARKS
SUPERVISORY PATENT EXAMINER